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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,892	09/17/2003	Hong-Yi Hubert Chen	MP0393	9088

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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/666,892	CHEN ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-23,25,26 and 51-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-23,25,26 and 51-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on April 10, 2007. Claims 1, 12-14 and 25 are currently amended; and none of the claims are currently cancelled or newly added. Therefore, claims 1-10, 12-23, 25-26 and 51-79 are currently pending in the application.

2. Applicant's arguments filed on April 10, 2007 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shelor (USPN: 7,024,544).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-10, 12-23, 14-23 and 25-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 recites "A register file for a data processing system comprising: a unbanked memory unit ..., input ports ..., output ports ..., and an address encoder...." It is unclear how a register file, which is a data/software file, can

have hardware components such as unbanked memory unit, input/output ports and address encoder. Claims 2-10 and 12-13 are also rejected as they further limit the rejected base claim 1. Claim 14 also includes similar limitations as claim 1 and rejected for the same reasons as claim 1. Claims 15-23 and 25-26 are also rejected as they further limit the rejected base claim 14.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10, 14-23, 57-58 and 60-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar (USPN: 5,701,493) in view of Shelor (USPN: 7,024,544).

As per claim 1, Jaggar teaches a register file for a data processing system comprising a unbanked memory unit (i.e. the stack memory area) having a plurality of memory locations, each memory location being addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to at least one register (i.e. registers R0-R13 in Figs. 1 and 8) and processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one of the memory locations using an encoded

address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one of the memory locations addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8). Jaggar further teaches an (common) address encoder (i.e. the combination of components 12-20 in Fig. 8) for all input ports, the address encoder to provide an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8).

However, Jaggar does not teach about having a plurality of encoders, a respective one of them for each of the input ports as claimed. Shelor, on the other hand, teaches about having an address encoder (i.e. 280 in Fig. 3) for providing encoded address for accessing one of the memory locations (e.g. see Col. 6, lines 16-21 and Fig. 3). Shelor further discloses that a separate address encoder for each of the input ports (i.e. signal lines) may be provided (e.g. see Col. 6, lines 39-41). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to have a separate address encoder for each of the input port in the register file of Jaggar as taught by Shelor. In doing so, it increases the overall performance of the data processing system by providing the encoded addresses for all inputs in parallel compared to one by one. Therefore, it is being advantageous.

As per claim 2, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that a plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) correspond to the plurality of memory

locations of the unbanked memory unit, i.e. each register corresponds to one or more memory locations depending on the processor mode (e.g. see the abstract).

As per claim 3, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. registers R0-R13 in Figs. 1 and 8) is addressable by a corresponding encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) (e.g. see the abstract and Figs. 1 and 8).

As per claim 4, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that at least two registers are capable of being accessed in different processor modes using the same encoded address, i.e. the system mode re-uses the same set of registers as the user mode (e.g. see the abstract).

As per claim 5, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that the read and write requests need to be redirected whenever the mode is changed, therefore, the plurality of memory locations of the stack memory are discontinuous (e.g. see Col. 6, lines 51-61).

As per claim 6, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that a bit width of the plurality of memory locations (i.e. the stackable memory area) is scalable to any arbitrary bit width size (e.g. see Col. 6, lines 51-61).

As per claim 7, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that inputs (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) are received associated with at least one register (i.e. "reg add" in Fig. 8) and processor mode (i.e. "mode bits" in Fig. 8), and wherein at least one of the outputs (i.e. output in Fig. 8) is data from a register associated with an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) obtained from the received inputs (e.g. see Fig. 8).

As per claim 8, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that data is outputted from the unbanked memory unit (i.e. the stackable memory area) for at least two instructions, i.e. two different READ requests/instructions (e.g. see claim 15).

As per claim 9, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that inputs (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) are received associated with at least one register (i.e. "reg add" in Fig. 8) and processor mode (i.e. "mode bits" in Fig. 8), and wherein one of the inputs is data to be written in a register associated with an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) obtained from the received inputs (e.g. see Fig. 8).

As per claim 10, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that data for at least two

retired instructions (i.e. WB 660 in Fig. 6) is to be written in at least two registers (i.e. via bus 426 in Fig. 6) (e.g. see Fig. 6 and paragraphs [0038]-[0040]).

As per claims 51, 61, 64, 74 and 78, see argument with respect to the rejection of claim 1. Claims 51, 61, 64, 74 and 78 are also rejected based on the same rationale as the rejection of claim 1.

As per claims 14-23, see arguments with respect to the rejection of claims 1-10, respectively. Claims 14-23 are also rejected based on the same rationale as the rejection of claims 1-10, respectively.

As per claims 52-56, see arguments with respect to the rejection of claims 2-6, respectively. Claims 52-56 are also rejected based on the same rationale as the rejection of claims 2-6, respectively.

As per claim 57, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that each address encoder (i.e. the combination of components 12-20 in Fig. 8) includes input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs associated with at least one register (i.e. "reg add" in Fig. 8) and processor mode (i.e. "mode bits" in Fig. 8) in providing a corresponding encoded address (e.g. see Fig. 8). Shelor also teaches that each address encoder (i.e. 280 in Fig. 3) includes input ports to receive inputs associated with at least one register (i.e. "register select bits" in Fig. 4) and processor mode (i.e. "mode select bits" in Fig. 4) in providing a corresponding encoded address (e.g. see Fig. 4).

As per claim 58, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Shelor teaches that each address encoder (i.e. 280 in Fig. 3) includes logic circuitry (i.e. the gate array shown in Fig. 4) to obtain the corresponding encoded address based on the received inputs (e.g. see Fig. 4).

As per claim 59, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Shelor disclose that the logic circuitry includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA) (i.e. the gate array shown in Fig. 4).

As per claim 60, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor is at least one of an embedded processor and a microprocessor (i.e. 62 in Fig. 8).

As per claims 62-63 and 67-69, see arguments with respect to the rejection of claims 2-6, respectively. Claims 62-63 and 67-69 are also rejected based on the same rationale as the rejection of claims 2-6, respectively.

As per claims 65-66, see arguments with respect to the rejection of claims 2-3, respectively. Claims 65-66 are also rejected based on the same rationale as the rejection of claims 2-3, respectively.

As per claims 70-73, see arguments with respect to the rejection of claims 57-60, respectively. Claims 70-73 are also rejected based on the same rationale as the rejection of claims 57-60, respectively.

As per claims 75-77 and 79, see arguments with respect to the rejection of claims 8-10 and 8, respectively. Claims 75-77 and 79 are also rejected based on the same rationale as the rejection of claims 8-10 and 8, respectively.

5. Claims 12-13 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view Shelor, further in view of Meier et al. (USPN: 6,363,471) hereinafter, Meier.

As per claims 12 and 13, the combination of Jaggar and Shelor teaches the claimed invention as described above, but failed to teach a latch circuit and a selector as clamed. Meier, however, teaches about using the latch or other clocked storage devices to store the intermediate values for pipelining to the next stage (e.g. see Col. 16, lines 21-35 and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Meier's latch circuit in the register file taught by the combination of Jaggar and Shelor. In doing so, this latch circuit can buffer the data (i.e. the encoded addresses) for pipeline storage in case if the data can be reused. The further limitation of having the selector coupled to the latch and the address encoder is well-known and notorious old in the art at the time of the current invention was made. By using the selector, such as a mux, the encoded address can be selected either from the latch circuit or directly from the address encoder based on a select signal. The Examiner herein taking Official Notice on this subject matter.

As per claims 25-26, see arguments with respect to the rejection of claims 12-13, respectively. Claims 25-26 are also rejected based on the same rationale as the rejection of claims 12-13, respectively.

Remarks

6. As to the remark, Applicant asserted that the specification of the current application does support the term "register file" as used in claims; and therefore, the 112, 1st rejection should be withdrawn.

Examiner respectfully traverses Applicant's remark for the following reasons:

The quoted phrases, submitted by Applicant, from the paragraphs [0002] and [004] of the current application is not supporting that the "register file" includes the hardware components included in the current claims. Therefore, 112, 1st rejection is maintained.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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